REMARKS

Applicants wish to thank the Examiner for the attention accorded to the instant application.

Claims 11-19 are pending in the application. Applicants have added new claims 20-26. Applicants have amended claim 11.

I. Specification Objections

The Examiner has objected to the Specification for various informalities.

Regarding the objection to the Specification in page 2, line 2, Applicants respectfully submit that the noted objection was addressed by a specification amendment in the prior Response to Office Action.

Regarding the other objections to the Specification, Applicants call attention to the amendments to the Specification. Applicants respectfully submit that the objections to the specification have been addressed, and the objections should be withdrawn.

II. Claim Rejections – 35 U.S.C. §112

The Examiner has rejected claims 11-19 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention.

¶6.1 Applicants respectfully traverse with respect to claim 11. Applicants respectfully submit that isolation of hardware and software elements is properly described in the specification

(see e.g., page 2 lines 5-7, page 2 line 17- page 3 line 18). The specification makes clear that, both in the prior art and in the present invention, the isolation of hardware elements and software elements is performed by an iterative process. Indeed, one of the goals of the invention is to shorten the time required for cooperative verification (that is, simulation of hardware and software elements in an LSI design together (see e.g., page 3 lines 9-18)). As stated in the Specification, the isolation of software and hardware elements (i.e. how much of the function of the LSI device will be performed by hardware versus how much of the function will be performed by software) will vary with respect to the aims of each hardware/software architecture designer according to varied design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.).

¶6.2 - ¶6.4 Applicants respectfully traverse with respect to claims 12-14. Support for the recited limitations of "isolating" and "structuring" source code elements are present in the original filed specification in Figure 1 (A3 and A16) and the passage from page 2 line 17 to page 3 line 18.

¶7.1 Applicants respectfully traverse with respect to claim 15. Applicants respectfully submit that isolation of hardware and software elements is properly described in the specification (see e.g., page 2, lines 5-7). Additionally, the isolation of the hardware and software elements is performed by experimentation since this is an iterative process during the architectural design of the LSI device. Applicants respectfully submit that the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.).

It is well settled that an "inventor need not, however, explain every detail since he is speaking to those skilled in the art." In re Howarth, 654 F.2d 103, 105 (CCPA 1981). Additionally, "not every last detail is to be described, else patent specifications would turn into production specifications, which they were never intended to be." In re Gay, 309 F.2d 769, 774 (CCPA 1962). Applicants respectfully request withdrawal of the rejections.

III. Claim Rejections – 35 U.S.C. §102

The Examiner has rejected claims 11-15 and 17-19 under 35 U.S.C. §102(b) as being anticipated by Tammemae et al. ("AKKA: a Tool-Kit for Cosynthesis and Prototyping").

Applicants have amended claim 11 to more particularly point out and distinctly claim the subject matter regarded as the invention. In particular, claim 11 has been amended to recite the additional step of "in response to said performance evaluation, modifying the configuration of said bus." The present invention, as recited in amended independent claim 11, is directed to software can be used to model and to evaluate the performance of hardware and software that is used to design an LSI device. As a result, in the simulation and evaluation phase, software units represent both software design elements and hardware design elements. The performance of this simulation program is then evaluated using an evaluation function that counts traffic using a software unit of the simulation program called a "bus" (a software bus connecting software units) that interconnects the software modules that model hardware components with the software modules that model software. (see, for e.g., Specification, page 4, lines 5-13). According to an aspect of Applicant's invention, this software unit, called the bus, is used for counting traffic to evaluate the overall design. (specification, page 4, lines 5-13.). Importantly, depending on the

performance, at a simulation stage, of the bus, the bus configuration can be modified and the simulation executed again. Particularly, the method of the present invention is used to evaluate the proper software and hardware separation of the design to produce optimal separation between the hardware and software elements. The optimization will vary, for example, with respect to the aims of each hardware/software architecture designer according to various design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.).

Tammemae is directed to a toolkit for the co-synthesis and prototyping of re-configurable and dedicated hardware. Tammemae teaches including data transfer profiling, such that for each variable access by the hardware element, a call to a counter function is made, and thereby each variable access is kept track of and counted. Importantly, Tammemae discloses a 32 bit bus for the data transfer between hardware and software elements. Tammemae does not teach or suggest modifying the bus at the simulation stage. Therefore, Tammemae does not teach or suggest the limitation of "in response to said performance evaluation, modifying the configuration of said bus."

Since the cited reference does not disclose each and every limitation recited in the amended claims, Applicants submit that independent claim 11 is allowable over the cited reference. Early notice to that effect is earnestly solicited. Claims 12-15 and 17-19, by their dependency on independent claim 11, are similarly allowable.

IV. Claim Rejections – 35 U.S.C. §103

The Examiner has rejected claim 16 under 35 U.S.C. §103(a) as being unpatentable over Tammemae in view of U.S. Patent No. 5,604,895 to Raimi et al. and Adams et al. ("Execution Time Profiling for Multiple Process Behavioral Synthesis").

Claim 16 is dependent from claim 11 and includes the step of "in response to said performance evaluation, modifying the configuration of said bus." As discussed above, Tammemae does not disclose, let alone teach or suggest, the modification of a bus between the hardware and software elements in response to a performance evaluation.

Neither Raimi nor Adams overcome the shortcomings of the Tammemae reference. Raimi is directed to a test coverage method. Importantly, Raimi does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11. In fact, Raimi teaches that isolation between hardware and software elements are defined by "known" parameters. Similarly, Adams does not overcome the shortcomings of the Tammemae reference. Adams teaches sequential reading of lines of source code for syntax analysis. However, Adams does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11.

Therefore, Applicants respectfully submit that a combination of Tammemae, Raimi and Adams does not teach or suggest every claimed feature of the invention. The prior art reference (or references) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Since a prima facie case of obviousness has not been set forth, Applicants respectfully submits that claim 11 is allowable over the cited references. Claim 16, by its dependency on claim 11, is similarly allowable.

V. New Claims

Applicants have added new claims 20-26. Independent claim 20 includes the step of "determining whether a line of source code represents writing data onto the bus to be evaluated." Such a step if not taught or suggested by Tammemae.

Tammemae is directed to a toolkit for the co-synthesis and prototyping of re-configurable and dedicated hardware. Tammemae teaches including data transfer profiling, such that for each variable access by the hardware element, a call to a counter function is made, and thereby each variable access is kept track of and counted. Importantly, Tammemae discloses a 32 bit bus for the data transfer between hardware and software elements. Tammemae does not teach or suggest modifying the bus at the simulation stage. Therefore, Tammemae does not teach or suggest the limitation of "determining whether a line of source code represents writing data onto the bus to be evaluated."

The combination of Tammemae, Raimi and Adams also does not disclose each and every limitation of claim 20. As discussed above, Tammemae does not disclose, let alone teach or suggest, the modification of a bus between the hardware and software elements in response to a performance evaluation.

Neither Raimi nor Adams overcome the shortcomings of the Tammemae reference. Raimi is directed to a test coverage method. Importantly, Raimi does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11. In fact, Raimi teaches that isolation between hardware and software elements are defined by "known" parameters. Similarly, Adams does not overcome the shortcomings of the Tammemae reference. Adams teaches sequential reading of lines of source code for syntax analysis. However, Adams does not teach or suggest a software bus between the

hardware and software elements of the simulation to exchange data traffic as required by claim 11.

Therefore, Applicants respectfully submit that a combination of Tammemae, Raimi and Adams does not teach or suggest every limitation of new claim 20. The prior art reference (or references) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Applicants respectfully submits that claim 20 is allowable over the cited references. Claims 21-26, by its dependency on claim 20, are similarly allowable.

VI. Conclusion

For the foregoing reasons, Applicants respectfully submit that all pending claims 11-19 are now in condition for allowance. Early notice to that effect is earnestly solicited.

Respectfully submitted,

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